said core of said first processor to said core of said second processor" and "a memory circuit for coupling said local memory of said first processor to said local memory of said second processor".

In contrast, the Asano reference discloses an apparatus having digital signal processor (DSP) modules (DMM's) 11a to 11k each comprising a DSP and its peripheral circuits. A control bus 12 connects together the task control unit 7 and the DMM's 11a to 11k. A memory bus 13 connects together the input frame memory 9 and the DMM's to 11a to 11k, and memory buses 14a to 14n connect together the common memories 10a to 10n and the DMM's 11a to 11k (col. 9, lines 46-53, Figs. 1 and 2).

Being that Asano teaches multiple DDM's (each having a DSP and its peripheral circuits), it fails to teach or suggest, "a first **processor for performing scalar processing**, said first processor comprising a core, a program memory and a local memory", "a second processor **for performing vector processing**, said second processor comprising a core, a program memory and a local memory", as required by Claim 6, since DSP are known to be ill suited for scalar processing. Only through improper hindsight would one of ordinary skill in the art be led to modify the Asano reference to re-engineer DDMs 11a to 11k such that one of the DSP in a DDM "performs scalar processing" and a second DSP in a second DDM "performs vector processing". Such modification would not be obvious without the improper hindsight provided by Applicants' disclosure. As a result, Claim 6 stands allowable.

New independent Claim 36 requires and positively recites, "a first processor comprising a core, a program memory and a local memory", "a second processor comprising a core, a program memory and a local memory", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said first processor to said local memory of said second processor**".

Asano further discloses that common memories 1 to n (10a - 10n) are connected to the DMM's to store locally decoded data or data which is being encoded and parameters (col. 9, lines 43-45 and Figures 1 & 2). As a result, Asano fails to teach or suggest, "**one and only one common memory coupling said local memory of said first processor to said local memory of said second processor**". Moreover, only through improper hindsight would one of ordinary skill in the

art be led to modify the Asano reference to re-engineer common memories 10a to 10n to instead be "one and only one memory", as required by Claim 36. There is no teaching in Asano, or the art for that matter, that would have led one of ordinary skill in the art to re-engineer Asano by removing common memories 10b-10n and instead have common memory 10a replace 10b-10n, without the improper hindsight provided by Applicants' disclosure. As a result, Claim 36 stands allowable.

New independent Claim 37 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

In contrast, the Asano reference discloses an apparatus having digital signal processor (DSP) modules (DMM's) 11a to 11k each comprising a DSP and its peripheral circuits. A control bus 12 connects together the task control unit 7 and the DMM's 11a to 11k. A memory bus 13 connects together the input frame memory 9 and the DMM's to 11a to 11k, and memory buses 14a to 14n connect together the common memories 10a to 10n and the DMM's 11a to 11k (col. 9, lines 46-53, Figs. 1 and 2).

Being that Asano teaches multiple DDM's (each having a DSP and its peripheral circuits), it fails to teach or suggest, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory", as required by Claim 37, since DSPs were known to be ill suited for protocol processing. Only through improper hindsight would one of ordinary skill in the art be led to modify the Asano reference to re-engineer DDMs 11a to 11k such that one of the DSPs in a DDM is a "main processor" and a second DSP in a second DDM is a "protocol processor". Such modification would not be obvious without the improper hindsight provided by Applicants' disclosure.

Further, Asano further discloses that common memories 1 to n (10a - 10n) are connected to the DMM's to store locally decoded data or data which is being encoded and parameters (col. 9, lines 43-45 and Figures 1 & 2). As a result, Asano fails to teach or suggest, "**one and only one**

common memory coupling said local memory of said first processor to said local memory of said second processor". Moreover, only through improper hindsight would one of ordinary skill in the art be led to modify the Asano reference to re-engineer common memories 10a to 10n to instead be "one and only one memory", as required by Claim 36. There is no teaching in Asano, or the art for that matter, that would have led one of ordinary skill in the art to re-engineer Asano by removing common memories 10b-10n and instead have common memory 10a replace 10b-10n, without the improper hindsight provided by Applicants' disclosure. As a result, Claim 37 stands allowable.

New independent Claim 38 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

In contrast, the Asano reference discloses an apparatus having digital signal processor (DSP) modules (DMM's) 11a to 11k each comprising a DSP and its peripheral circuits. A control bus 12 connects together the task control unit 7 and the DMM's 11a to 11k. A memory bus 13 connects together the input frame memory 9 and the DMM's to 11a to 11k, and memory buses 14a to 14n connect together the common memories 10a to 10n and the DMM's 11a to 11k (col. 9, lines 46-53, Figs. 1 and 2).

Being that Asano teaches multiple DDM's (each having a DSP and its peripheral circuits), it fails to teach or suggest, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited** ", as required by Claim 38, since DSPs were known to be ill suited for protocol processing. Only through improper hindsight would one of ordinary skill in the art be led to modify the Asano reference to re-engineer DDMs 11a to 11k such that one of the DSPs in a DDM is a "main processor" and a second DSP in a second DDM is a "protocol processor". Such modification would not be obvious without the improper hindsight provided by Applicants' disclosure. As a result, Claim 38 stands allowable.

New independent Claim 39 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

In contrast, the Asano reference discloses an apparatus having digital signal processor (DSP) modules (DMM's) 11a to 11k each comprising a DSP and its peripheral circuits. A control bus 12 connects together the task control unit 7 and the DMM's 11a to 11k. A memory bus 13 connects together the input frame memory 9 and the DMM's to 11a to 11k, and memory buses 14a to 14n connect together the common memories 10a to 10n and the DMM's 11a to 11k (col. 9, lines 46-53, Figs. 1 and 2).

Being that Asano teaches multiple DDM's (each having a DSP and its peripheral circuits), it fails to teach or suggest, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited** ", as required by Claim 38, since DSPs were known to be ill suited for protocol processing. Only through improper hindsight would one of ordinary skill in the art be led to modify the Asano reference to re-engineer DDMs 11a to 11k such that one of the DSPs in a DDM is a "main processor" and a second DSP in a second DDM is a "protocol processor". Such modification would not be obvious without the improper hindsight provided by Applicants' disclosure.

Further, Asano further discloses that common memories 1 to n (10a - 10n) are connected to the DMM's to store locally decoded data or data which is being encoded and parameters (col. 9, lines 43-45 and Figures 1 & 2). As a result, Asano fails to teach or suggest, "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**". Moreover, only through improper hindsight would one of ordinary skill in the art be led to modify the Asano reference to re-engineer common memories 10a to 10n to

instead be "one and only one memory", as required by Claim 39. There is no teaching in Asano, or the art for that matter, that would have led one of ordinary skill in the art to re-engineer Asano by removing common memories 10b-10n and instead have common memory 10a replace 10b-10n, without the improper hindsight provided by Applicants' disclosure. As a result, Claim 39 stands allowable.

Claims 7-19 stand allowable as depending from allowable claims and include further limitation not taught or suggested by the references of record.

Claim 7 further defines the apparatus of Claim 6, wherein said second processor is the main processor of said apparatus. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 8 further defines the apparatus of Claim 7, wherein said first processor is a microprocessor. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 7.

Claim 9 further defines the apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP". The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 7.

Claim 10 further defines the apparatus of Claim 6, wherein said program memory of said first processor is ROM memory. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 11 further defines the apparatus of Claim 6, wherein said local memory of said first processor is RAM memory. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 12 further defines the apparatus of Claim 6, wherein said program memory of said second processor is ROM memory. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 13 further defines the apparatus of Claim 6, wherein said local memory of said second processor is RAM memory. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 14 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 15 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 16 further defines the apparatus of Claim 6, wherein said second processor is a protocol processor. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 17 further defines the apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

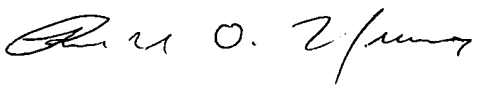
Claim 18 further defines the apparatus of Claim 6, wherein said second processor comprises: an incremental register; and a program memory connected to the incremental register.

The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 19 further defines the apparatus of Claim 6, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions: integers corresponding to arithmetic and logic operations on integer numbers; transfer corresponding to the transfer operations between a register in said protocol processor and memory; and monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claims 6-19 and 34-39 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



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